FIG. 11 shows an embodiment of a memory cell including a transistor **97** and a capacitor element **98**. In such a memory cell, the dummy elements as described above can be used for transistors and capacitor elements.

For example, in the case of a transistor, a gate electrode **121** on a substrate **120** corresponds to the top electrode in a capacitor element as shown in FIG. **13**. A gate insulating layer (not shown in FIG. **13**) corresponding to a capacitor dielectric layer in a capacitor element is formed between the substrate **120** and the gate electrode **121**. When forming a transistor, a dummy gate electrode **122** can suppress the degradation of the transistor as is in the case of a capacitor element. As shown in FIG. **13**, a source electrode **123** and a drain electrode **124** formed in the substrate **120** is not necessary below the dummy gate electrode **122**.

In the memory cell in FIG. **11**, a transistor **97** includes a gate **87**, a source **85**, a drain **86** and a gate insulating layer **88** composed of a ferroelectric material. The memory cell also has a capacitor element **98** including a bottom electrode **91**, a capacitor insulating layer **92** composed of a ferroelectric material and a top electrode **93**.

The transistor **97** and the capacitor element **98** are connected with other elements by bit lines **89**, **90** and **95**. A field oxide layer **82** and insulating layers **83** and **84** formed on a substrate **81** prevent unnecessary contacts between the elements.

A memory cell in FIG. **12** also has transistors **117** including gates **107**, sources **105**, drains **106**, gate insulators **103** and gate insulating layers **108** composed of a ferroelectric material. On an insulating layer **102**, there are capacitor elements **118** including bottom electrodes **111**, capacitor insulating layers **112** composed of a ferroelectric material and top electrodes **113**.

The transistor **117** and the capacitor element **118** also are connected with each other and other elements by bit lines **109**, **110** and **115**. Insulating layers **102** and **104** prevent unnecessary contacts between the elements. In the memory cells as shown in FIGS. **11** and **12**, dummy capacitor elements and/or dummy transistors (dummy gate electrodes) can be used for preventing degradation of the layer composed of the dielectric with high dielectric constant.

The semiconductor device for which the dummy element can be used is not limited to the memory cells as described above.

EXAMPLE

The devices as shown in FIGS. **14** to **16** were produced. In the semiconductor device, capacitor elements **61**, first dummy capacitor elements **62** and second dummy capacitor elements **63** were arranged on a substrate **60**.

As shown in FIGS. **14** and **15**, in the capacitor elements **61** and the first dummy capacitor elements **62**, a first electrode **64** and a first dummy electrode **67** are included in the same electrically conductive film. A capacitor dielectric layer **65** and a dummy capacitor dielectric layer **68** also are included in the same dielectric film. As shown in FIG. **15**, the first dummy capacitor elements **62** are located at the end of the line including the capacitor elements **61** and the first dummy capacitor elements **62**.

As shown in FIGS. **14** and **16**, only the second dummy capacitor elements **63** are provided at the line at the end. In the second dummy capacitor elements **63**, first dummy electrodes **71** are included in the same electrically conductive film and dummy dielectric capacitor layers **72** are included in the same dielectric film.

The space α between a second electrode **66** and a second dummy electrode **69** in the first dummy capacitor element **62** was set at 1.5 μm. The space β between the second electrode **66** and a second dummy electrode **73** in the second dummy capacitor element **63** was set at 12.8 μm. The devices were produced by the process as described above. The capacitor dielectric layer was composed of SrBixTaxOy at a thickness of 0.24 μm. The electrodes were composed of Pt.

On the other hand, semiconductor devices were produced in the same way but without the first dummy elements **62** and the second dummy elements **63**. Remnant polarization in each device was measured.

As shown in FIG. **17**, remnant polarization in the devices with the dummy elements was 13 $\mu C/cm^2$ to 15 $\mu C/cm^2$. As shown in FIG. **18**, remnant polarization in the devices without the dummy elements was 5 $\mu C/cm^2$ to 10 $\mu C/cm^2$. Thus, the dummy elements can improve and stabilize remnant polarization in the capacitor elements. Therefore, for example, the dummy elements can expand a margin for error in reading data from the device.

The relationship between the space β and the remnant polarization was investigated. As shown in FIG. **19**, when the space β was above 14 μm, the remnant polarization sharply dropped (line A). In this case, the size of the second electrodes **66** and the second dummy electrodes **69** and **73** were 5×5 μm. When the size of the electrodes was set at 1.5×1.5 μm, the remnant polarization sharply dropped in the range above 9 μm. When the size of the electrodes was set at 1×1 μm, the remnant polarization sharply dropped in the range above 5 μm. The space β below 0.3 μm makes it difficult to produce the elements. The same results were observed when the space α was changed instead of the space β.

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The embodiments disclosed in this application are to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description, all changes that come within the meaning and range of equivalency of the claims are intended to be embraced therein.

What is claimed is:

1. A semiconductor device comprising:

a substrate,

a semiconductor element on the substrate, the semiconductor element including a first dielectric layer and an electrode on the first dielectric layer, and

a dummy semiconductor element on the substrate, the dummy semiconductor element including a second dielectric layer and a dummy electrode on the second dielectric layer,

wherein the dummy semiconductor element is located so that a space between the electrode and the dummy electrode is in a predetermined range, and the semiconductor device is a transistor in which the electrode works as a gate electrode of the transistor; and said first dielectric layer is composed of the material selected from a dielectric material having a dielectric constant of 100 or more and a ferroelectric material.

2. A semiconductor device according to claim **1**, wherein the predetermined range of the space is between 0.3 μm and 14 μm.

3. A semiconductor device according to claim **1**, wherein the electrode and the dummy electrode are composed of the same electrically conductive material.

4. A semiconductor device according to claim **1**, wherein the first dielectric layer and the second dielectric layer are composed of the same dielectric material.

5. A semiconductor device according to claim **1**, wherein the electrode is surrounded by the dummy electrode.

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